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Mitigation of Lower Order Harmonics with Filtered Svpwm In Multiphase Voltage Source Inverters

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Abstract
Multi-phase machines and drives is a topic of growing relevance in recent years, and it presents many challenging issues that still need further research. This is the case of multi-phase space vector pulse width modulation (SVPWM), which shows not only more space vectors than the standard three-phase case, but also new subspaces where the space vectors are mapped. In the digital implementation, multiphase reference voltages are sampled and fed into the digital modulator to produce gating signals at a constant clock rate f. This means a finite pulse-width resolution because the gating state transition can only occur at some specific time instants depending on frequency. This results in a deviation of produced phase voltages from the desired phase voltages, i.e., increasing harmonic distortion especially for a small modulation index signal.
In the present paper a filtered space-vector pulse-width modulation (SVPWM) considering finite pulse-width resolution is proposed to produce a switching sequence with reduced baseband harmonics for multiphase voltage source inverters (VSI). This is achieved by incorporating a pseudo feedback loop regarding weighted voltage difference between desired and produced phase voltages.
Keywords: - SVPWM, Voltage Source inverters, Harmonic Distortion.

I. INTRODUCTION

Various Pulse Width Modulation techniques like Single-pulse modulation Multiple pulse modulation, Sinusoidal pulse width modulation, (Carrier based Pulse Width Modulation Technique) are employed in modern days because of their flexibility and higher efficeinecy.Various pulse-width modulations (PWM) such as third harmonic injection PWM , zero-sequence injection PWM, space-vector PWM (SVPWM), and unified PWM have been proposed to generate the control commands of three-phase voltage source inverter (VSI) for ac variable speed drives.

In recent years, multiphase PWMs have been proposed because of their increased efficiency, reduced torque pulsation, improved fault tolerance, and lower power handling requirement by adopting multiphase machines.

In the digital implementation, multiphase reference voltages are sampled and fed into the digital modulator to produce gating signals at a constant clock rate *f*. This means a finite pulse-width resolution because the gating state transition can only occur at some specific time instants depending on *f*. This will result in a deviation of produced phase voltages from the desired phase voltages, i.e., increasing harmonic distortion especially for a small modulation index signal. For example, when system master clock frequency and reference sampling frequency are given as 48 and 3 kHz, respectively, the maximum refreshing rate of gating signals is f = 48 kHz and the pulse-width resolution is 4-bit within each input period ($48k = 3k \times 24$). Thus, the worst-case rounding error for the duty ratio is 1/32 = 0.03125. For small modulation index, the effect of error on signal distortion becomes quite significant. Further, if a 16-bit pulse-width resolution is desired, the master clock needed is 196.61MHz for 3 kHz reference sampling frequency and is about 1.31 GHz for ultrasonic carrier. This will increase the cost and power consumption of the devices.

To alleviate the adverse effect induced by finite pulse-width resolution, proposals were reported to achieve higher precision of duty ratios without increasing clock rate. In, a single-phase PWM to regulate a dc voltage command was proposed by using an error accumulator and lookup tables. A feedback quantization scheme proposed for three-phase VSI spreads the spectrum of the produced phase currents/voltages in a wide frequency band. The general solution using SVPWM for multiphase VSIs was reported. The multiphase SVPWM was formulated as a matching problem between the reference and the switching waveform without

considering the finite pulse-width resolution.

In this study, the frequency-weighted error due to finite resolution is considered in the objective function to emphasize the quality of in-band signal matching. The frequency weighting is realized by filtering the error signals. This results in a multiple-input–multiple-output (MIMO) pseudo feedback architecture. Based on similar analysis, the block diagram for VSI systems of any phase number can be obtained.

II. MULTIPHASE VSI FILTERED SVPWM WITH FEEDBACK

A. *Multiphase Voltage Source Inverter:*

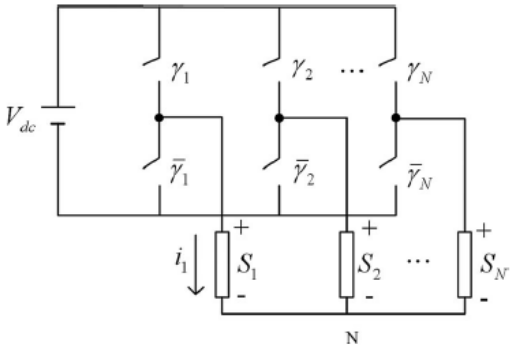


Fig. 1. N-phase VSI topology

Fig. 1 depicts the simplified structure of an *N*-phase VSI where $S_1, S_2, \ldots, S_N$ are the output phase voltages of the inverter (with reference to the neutral point). Two switching states exist in one phase leg: only the upper or the lower switch is turned ON. The switching state is denoted as +1 (0) when the upper (lower) switch of the phase leg is turned ON. Then, the gating states can be represented by a vector $\mathrm{s} = [s_1\ s_2 \cdots s_N]^T$ where $s_1, s_2, \ldots, s_N \in \{0,1\}$ are the states of phase legs. Equation (1) gives the relationship between phase voltage vector, $\mathrm{S} = [S_1\ S_2 \cdots S_N]^T$, and the gating state. Notably, for an *N*-phase VSI, 2*N* gating states exist and each corresponds to a different phase voltage vector (also called a space vector) except for two zero switching states, $\mathrm{s} = [0 \cdots 0]T$ and $\mathrm{s} = [1 \cdots 1]^T$

$$\mathrm{S} = \begin{bmatrix} S_1 \\ S_2 \\ \vdots \\ S_N \end{bmatrix} = \begin{bmatrix} (N-1)/N & -1/N & \cdots & -1/N \\ -1/N & (N-1)/N & \ddots & \vdots \\ \vdots & \ddots & \ddots & -1/N \\ -1/N & \cdots & -1/N & (N-1)/N \end{bmatrix} \times \begin{bmatrix} s_1 \\ s_2 \\ \vdots \\ s_N \end{bmatrix} \triangleq \mathrm{S}_c\mathrm{s} \tag{1}$$

Remark 1: Multiplying $[1 \cdots 1]$ on both sides of (1), we obtain that the phase voltage vector produced by the N-phase VSI (for the y-connected load) must satisfy $\sum_{j=1}^{N} S_j = 0$.

B. *Signal Matching Objective:*

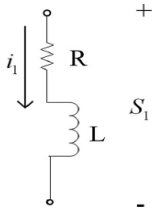


Fig.2. Model circuit of a winding of a motor

Given a desired phase voltage **r**, the objective of the modulator is to produce gating signals for VSI to recover the desired phase voltages on load windings. However, the phase voltages produced are restricted. For example, only seven different phase voltages can be produced by a three-phase VSI. Therefore, it is necessary to consider the characteristics of the load. The load is usually approximated by a serial-connected resistance and inductance circuit (refer to Fig. 2). The phase current is expressed by passing the produced phase voltage through a low-pass filter

$$\mathrm{P} = \left\{ \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}, \begin{bmatrix} 2/3 \\ -1/3 \\ -1/3 \end{bmatrix}, \begin{bmatrix} -1/3 \\ 2/3 \\ -1/3 \end{bmatrix}, \begin{bmatrix} -1/3 \\ -1/3 \\ 2/3 \end{bmatrix}, \begin{bmatrix} -2/3 \\ 1/3 \\ 1/3 \end{bmatrix}, \begin{bmatrix} 1/3 \\ -2/3 \\ 1/3 \end{bmatrix}, \begin{bmatrix} 1/3 \\ 1/3 \\ -2/3 \end{bmatrix} \right\}$$

$$i_1 = \frac{1}{sL + R} S_1 \tag{2}$$

For an *N*-phase sinusoidal reference input **r** with phase shift $2\pi/N$, it is intuitive that the desired phase currents are also *N*-phase sinusoidal waves. Therefore, the objective is to find the switching states (gating states) such that the produced phase voltages are sinusoidal waves after low-pass filtering or alternatively, the difference between desired and produced phase voltages within low frequency band shall be minimized.

C. *Problem Formulation:*

The *N*-dimensional desired phase voltage vector satisfying (3) can be written in the form $\mathrm{r} = [S^*_1\ S^*_2 \cdots S^*_N]^T$ where

$$S^*_1 + S^*_2 + \cdots + S^*_N = 0 \tag{3}$$

Assume that the controller input sampling frequency is f_c and that the pulse-width resolution within each input period is *b* bits, i.e., the controller outputs are updated at a rate $2^b \times f_c$ Hz. The average phase voltage produced on the windings within one input period is

$$\bar{\mathrm{v}}(k) = \frac{1}{2^b} \sum_{j=0}^{2^b-1} \mathrm{v}(j) = \frac{1}{2^b} \sum_{j=0}^{2^b-1} \mathrm{S}_c\mathrm{s}(j) \tag{4}$$

Where **v** (*j*), one of the space vectors, is the corresponding phase voltage vector induced by the *j*th selected gating state **s** (*j*) within one input period.

Note that the image of $\bar{v}$ is all possible linear combinations of 2^b basic vectors. The objective of the proposed modulator is to determine gating states (or **v** (*j*)) that minimizes filtered error power within each input period. The filtered error is represented as

$$\mathbf{E}(\mathbf{z}) = \mathbf{W}(z)\left(\mathbf{R}(z) - \bar{\mathbf{V}}(z)\right) \quad (5)$$

Where W(*z*) is an $N \times N$ filter matrix and R(*z*) ,$\bar{v}$(*z*) are z-transform of the elements in r, $\bar{v}$, respectively. A *p*th-order low pass filter, denoted as *w* (*z*), is selected as the weighting filter for each phase to enhance low-frequency-band performance, i.e., W(*z*) is a diagonal matrix with *w* (*z*), a single-input–single output (SISO) transfer function, on its diagonal terms. *w* (*z*) can be represented in the state-space form as

$$w(z) = d + \mathbf{c}(z\mathbf{I} - \mathbf{a})^{-1}\mathbf{b} \quad (6)$$

Where a $\in R^{p\times p}$, b $\in R^p$, c $\in R^{1\times p}$, and $d \in R$. Further, the state-space form of W (*z*) is

$$\mathbf{x}(k+1) = \mathbf{A}\mathbf{x}(k) + \mathbf{B}(\mathbf{r}(k) - \bar{\mathbf{v}}(k))$$
$$\mathbf{e}(k) = \mathbf{C}\mathbf{x}(k) + \mathbf{D}(\mathbf{r}(k) - \bar{\mathbf{v}}(k)) \quad (7)$$

Where e (*k*) $\in RN$ is the filtered error vector and **x** (*k*) $\in R^{pN}$ is a system state vector. Then, (A,B,C,D) can be written as

$$\mathbf{A} = \begin{bmatrix} \mathbf{a} & \mathbf{0}_a & \cdots & \mathbf{0}_a \\ \mathbf{0}_a & \mathbf{a} & \ddots & \vdots \\ \vdots & \ddots & \ddots & \mathbf{0}_a \\ \mathbf{0}_a & \cdots & \mathbf{0}_a & \mathbf{a} \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} \mathbf{b} & \mathbf{0}_b & \cdots & \mathbf{0}_b \\ \mathbf{0}_b & \mathbf{b} & \ddots & \vdots \\ \vdots & \ddots & \ddots & \mathbf{0}_b \\ \mathbf{0}_b & \cdots & \mathbf{0}_b & \mathbf{b} \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} \mathbf{c} & \mathbf{0}_c & \cdots & \mathbf{0}_c \\ \mathbf{0}_c & \mathbf{c} & \ddots & \vdots \\ \vdots & \ddots & \ddots & \mathbf{0}_c \\ \mathbf{0}_c & \cdots & \mathbf{0}_c & \mathbf{c} \end{bmatrix}, \text{ and } \mathbf{D} = \begin{bmatrix} d & 0 & \cdots & 0 \\ 0 & d & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & d \end{bmatrix}$$

Where $\mathbf{0}_a$, $\mathbf{0}_b$, and $\mathbf{0}_c$ are the zero matrices with dimensions $\mathbf{0}_a \in R^{p\times p}$, $\mathbf{0}_b \in R^p$, and $\mathbf{0}c \in R^{1\times p}$. The signal matching problem becomes

$$\min_{\mathbf{v}(j)\in \text{basic vectors}} \|\mathbf{e}(k)\|_2^2 = \min_{\mathbf{v}(j)\in \text{basic vectors}} \|\mathbf{C}\mathbf{x}(k) + \mathbf{D}\mathbf{r}(k) - \mathbf{D}\bar{\mathbf{v}}(k)\|_2^2 \quad (9)$$

Where $\bar{\mathbf{v}}(k) = \frac{1}{2^b}\sum_{j=0}^{2^b-1}\mathbf{S}_c\mathbf{s}(j)$.

III. PERFORMANCE ANALYSIS

A. *Range of λ and its Influence:*

The value of □ is fixed once λ is selected [refer to (22)]. To have feasible duties, elements of □, ρi , for $i = 1--N$, should be kept within the range $0 \le \rho i \le 1$. Therefore, the acceptable range of λ is limited. To see this, first define the permutation matrix $\mathbf{P}_M$ as

$$\mathbf{P}_M\mathbf{v}^*(k) = [\hat{v}_1 \quad \hat{v}_2 \quad \cdots \quad \hat{v}_N]^T$$

Such that $\hat{v}_1 \ge \hat{v}_2 \ge \cdots \ge \hat{v}_N$ (23)

Therefore

$$\mathbf{P}_M q_b\{\mathbf{v}^*(k) + \lambda\mathbf{d}\} = [\hat{\rho}_1 \quad \hat{\rho}_2 \quad \cdots \quad \hat{\rho}_N]^T \quad (24)$$

Where $\hat{\rho}_1 \ge \hat{\rho}_2 \ge \cdots \ge \hat{\rho}_N$. Then, the feasible range of ρi , for $i = 1--N$, is

$$\max(\mathbf{\Theta}) = \hat{\rho}_1 = q_b\{\hat{v}_1 + \lambda\mathbf{d}\} \le 1$$
$$\min(\mathbf{\Theta}) = \hat{\rho}_N = q_b\{\hat{v}_N + \lambda\mathbf{d}\} \ge 0 \quad (25)$$

Or alternatively, $-\hat{v}_N \le \lambda \le 1 - \hat{v}_1$ regardless of finite pulse width resolution, and $-\hat{v}_N + \frac{1}{2^{b+1}} \le \lambda \le 1 - \hat{v}_1 - \frac{1}{2^{b+1}}$ considering *b*-bit pulse-width resolution.

Applying the coefficient $\beta \in [0\ 1]$, λ can be written as

$$\lambda = (1-\beta)\left(-\hat{v}_N + \frac{1}{2^{b+1}}\right) + \beta\left(1 - \hat{v}_1 - \frac{1}{2^{b+1}}\right) \quad (26)$$

Remark 2: Refer to Fig. 4, 2*N* switching number occurs within one input period. When λ is selected as its boundary value, $-\hat{v}_N + \frac{1}{2^{b+1}}$ or $1 - \hat{v}_1 - \frac{1}{2^{b+1}}$, the switching number is reduced to 2 (N − 1) since either $\hat{\rho}_1 = 1$ or $\hat{\rho}_N = 0$ occurs which implies one phase leg staying at the same level during the whole input period.

B. *Minimum Total Conduction Time:*

The total conduction time is defined as the sum of duties of the active gating states applied within one input period. Minimum total conduction time implies the maximum modulation index. Note that for an *N*-phase VSI system, 2*N* gating states exist and two zero switching states, **s**0 and **s**2*N* −1, correspond to the same space vector, **S** = **0**Consider the permutated phase duty vector $\mathbf{P}_M$□ [see (22) and (24)]. It is intuitive that the maximum duties for $\mathbf{s}_0$ and $\mathbf{s}_2N$ −1 are $1 - \hat{\rho}_1$ and $\hat{\rho}_N$, respectively. Therefore, the minimum total conduction time is obtained by subtracting the duty of $\mathbf{s}_2N$ −1 from the maximum duty among phase legs $\hat{\rho}_1 - \hat{\rho}_N$.

Remark 3: From *remark 2*, give $\lambda = -\hat{v}_N + \frac{1}{2^{b+1}}$ or 1 – $\hat{v}_1 - \frac{1}{2^{b+1}}$, and the modulator has minimum switching number 2 (N − 1). Therefore, the proposed gating signal generator operates at minimum total conduction time and minimum switching number point, yielding a maximum modulation index and minimum switching loss.

C. *Quantization Error:*

The quantization error vector □b is defined as the difference between input and output of the quantizer qb {.} which is the same as the conventional methods, i.e. (refer to Fig. 3)

$$\boldsymbol{\Delta}_b = (\mathbf{v}^* + \lambda \mathbf{d}) - q_b \{(\mathbf{v}^* + \lambda \mathbf{d})\} \quad (27)$$

The concept of error analysis is extended to the MIMO system. **e** in (7) is written as the following expression using (9) and (10) and Fig. 3:

$$\begin{aligned} \mathbf{e}(k) &= \mathbf{C}\mathbf{x}(k) + \mathbf{D}(\mathbf{r}(k) - \bar{\mathbf{v}}(k)) \\ &= \mathbf{C}\mathbf{x}(k) + \mathbf{D}\mathbf{r}(k) - \mathbf{D}\mathbf{S}_c q_b \{\mathbf{v}^*(k) + \lambda \mathbf{d}\} \\ &= \mathbf{D}(\mathbf{v}^*(k) - \mathbf{S}_c q_b \{\mathbf{v}^*(k) + \lambda \mathbf{d}\}) \end{aligned} \quad (28)$$

Then from (27), (28) becomes

$$\begin{aligned} \mathbf{e}(k) &= \mathbf{D}(\mathbf{v}^*(k) - \mathbf{S}_c q_b \{\mathbf{v}^*(k) + \lambda \mathbf{d}\}) \\ &= \mathbf{D}(\mathbf{v}^*(k) - \mathbf{S}_c(\mathbf{v}^*(k) + \lambda \mathbf{d} - \boldsymbol{\Delta}_b)) \\ &= \mathbf{D}(\mathbf{v}^*(k) - (\mathbf{v}^*(k) - \mathbf{S}_c \boldsymbol{\Delta}_b)) \\ &= \mathbf{D}\mathbf{S}_c \boldsymbol{\Delta}_b \end{aligned} \quad (29)$$

Therefore, the signal e is dependent on the quantization error Δ_b. Notably, the portion $S_c\Delta_b$ is the influence of quantization error Δb on the load. Further, because the filter matrix is in diagonal form, D is a diagonal matrix, i.e., e is the scaled quantization error that appears on the load windings and is minimized by the proposed modulator.

IV. MATLAB DESIGN OF CASE STUDY

Simulation that compares the influence of filter matrix is done under the five-phase setting. MATLAB is used as a simulation platform. Five-phase sinusoidal references with large/small modulation indices are applied to verify the compensating ability of the proposed switching strategy.

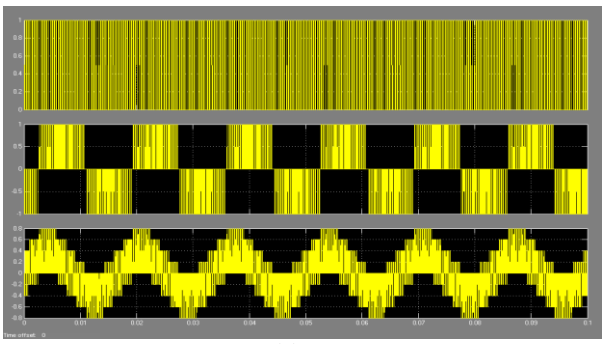
The modulator with first- and second-order weighting filters is compared with the conventional SVPWM under the digital implementation settings. The weighting filters are the first- and second-order integrator systems, z/(z - 1) and z 2 /(z- 2z +1). We denote the one having no feedback loop as SVPWM. The system state-space matrices for the first- and second-order filter matrices are a = b = c = d =1(denoted as PWM_1st) . Referring to Fig. 3, the implementation block diagram is shown in Fig. 5. Notably, no multipliers are needed in the implementation. Because the coefficients of filters are either 1 or 2, only adders and shifters are needed to implement weighting filter.

V. SIMULATION RESULTS

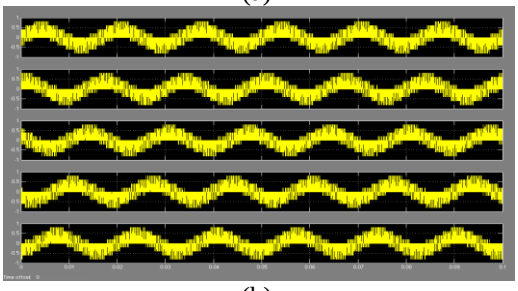
A five-phase sinusoidal reference input with normalized amplitude 0.51 and frequency 60 Hz is applied. The carrier frequency is 3 kHz and the pulse-width resolution is 8, yielding a clock rate of $2^8 \times 3k = 768kHz$. Figs. 7(a)–8(a) show one of the leg voltages, line-to-line voltages, and phase voltages for the aforementioned PWMs. The five-phase voltages produced on the load are also shown in Figs. 7(b)–8(b) to verify the correctness of the gating signals. To have a precise comparison, Tables I lists the switching number and the harmonic distortion for modulation indices 0.51. It is seen that with the shaping filter that relocates the noise in the higher frequency band, the harmonic distortion of PWM_1st is reduced within [0 500] Hz compared to that of SVPWM, especially for small modulation indexThe harmonic distortion within [0 5 k] Hz for these systems is comparable yielding approximately the same level of error power which is induced by finite pulse-width resolution. Therefore, with the shaping filter, components of error tend to be distributed over high-frequency band.

TABLE I- HARMONIC DISTORTION AND SWITCHING NUMBER FOR 8-BIT PULSE-WIDTH RESOLUTION (WITH INPUT AMPLITUDE 0.51)

Input amplitude: 0.51	SVPWM	PWM_1st
Harmonics distortion within [0 500] Hz (%)	0.439	0.244
Harmonics distortion within [0 5000] Hz (%)	43.072	43.150
Switching number (per second)	24k	24k

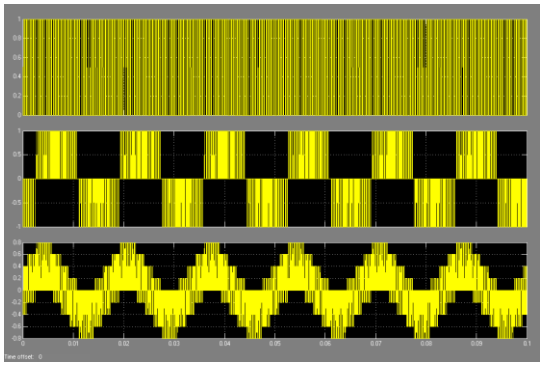


(a)

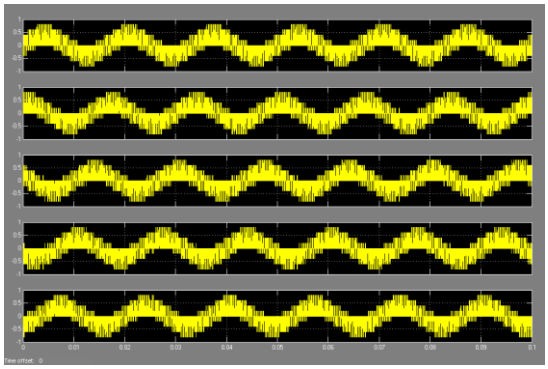


(b)

Fig. 7. Simulation results of SVPWM. (a) Leg voltage (top), line-to line voltage (middle), and phase voltage (bottom). (b) Five-phase load voltages.



(a)



(b)

Fig. 8. Simulation results of PWM_1st. (a) Leg voltage (top), line-to-line voltage (middle), and phase voltage (bottom). (b) Five-phase load voltages.

VI. CONCLUSION

In the present paper a filtered space-vector pulse-width modulation (SVPWM) considering finite pulse-width resolution has been proposed to produce a switching sequence with reduced baseband harmonics for multiphase voltage source inverters (VSI). This is achieved by incorporating a pseudo feedback loop regarding weighted voltage difference between desired and produced phase voltages.

The simulation results state that SVPWM is sensitive to the pulse-width resolution. By applying the feedback loop with weighting filter, the harmonic distortion is reduced compared with conventional SVPWM. Furthermore the results indicate that the proposed model is capable of providing satisfactory performance at low frequencies particularly.

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